A Real-Time Infrared Scene Simulator in CMOS/SOI MEMS

Jeremy D. Popp, Bruce Offord, and Richard Bates
SSC San Diego

H. Ronald Marlin and Chris Hutchens
Titan Systems Corporation

Derek Huang
Advanced Analog VLSI Design Center

ABSTRACT
A 64 x 128 real-time infrared (RTIR) complementary metal-oxide semiconductor (CMOS)/ silicon-on-insulator (SOI) scene generation integrated circuit (IC) is described. The RTIR IC offers real-time dynamic thermal scene generation. This system is a mixed-mode design, with analog scene information written and stored into a thermal pixel array. The design uses micro-electro-mechanical sensors (MEMS) in conjunction with SSC San Diego's 0.8-μm CMOS/SOI process to develop a RTIR IC scene generator.

INTRODUCTION

The objective of the real-time infrared (RTIR) project is to develop a reliable prototype infrared (IR) test set for use in calibration and testing of IR systems, including built-in-test to ensure the real-time reliability of IR sensing systems. The potential of RTIR as built-in-test equipment (BITE) is to improve the reliability of IR sensors, thus lowering the overall system cost of operation. Infrared scene simulators that use bulk complementary metal-oxide semiconductor (CMOS)/micro-electromechanical systems (MEMS) have been reported previously [1]; however, this work uses silicon-on-insulator (SOI) as the starting material. The MEMS area is scaled down to create higher density pixel arrays, with low leakage at higher temperatures.

DESIGN

The integrated circuit (IC) consists of a data input block, address write control, and pixel-specific electronics including a microheater suspended over a micromachined cavity in the silicon substrate. The display IC consists of an array of 64 x 128 thermally isolated, resistive emitters. The thermal pixel array (TPA) elements have response times less than a millisecond, making them suitable for real-time scene simulation. The pixel cell contains a resistive heater element (or infrared emitter), a storage capacitor, pixel drive transistors, and switches (Figure 1). The user digitally specifies a specific row and column and then writes a pixel voltage to the desired cell via the analog multiplexer (MUX). The infrared pixel array IC is designed for use with a computer or an electronic controller to service or update the real-time images. The computer sends gray-scale scene data to the pixel array in the form of voltages, which the TPA displays as a gray-scale image. The computer controls digital row and column address lines and writes the analog inputs via a digital-to-analog converter (DAC) to the RTIR IC. The voltage magnitude reflects the desired IR intensity of the pixel element, thereby achieving the gray-scale levels. After writing to the pixel, the desired voltage is stored dynamically by Chold, producing the desired IR pixel intensity while the remaining pixels are updated. The pixel electronics of the array are designed to exploit the low leakage properties of SOI during high-temperature operation. Voltage droop is the greatest problem affecting pixel dynamic range and accuracy. Droop is primarily a result of the leakage currents through

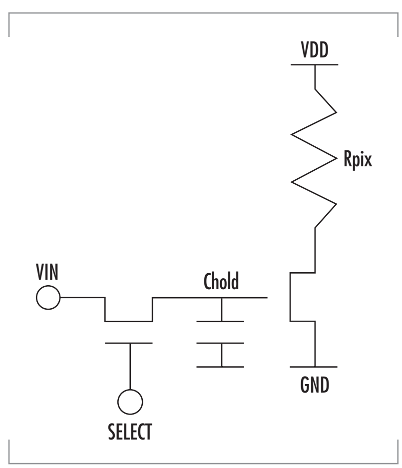

FIGURE 1. Pixel schematic: the drive transistor is a BTS device; the access transistor is an HGATE device.

Report Documentation Page

Form Approved
OMB No. 0704-0188

1. REPORT DATE	2. REPORT TYPE	3. DATES COVERED
AUG 2001		-

4. TITLE AND SUBTITLE	
A Real-Time Infrared Scene Simulator in CMOS/SOI MEMS	5a. CONTRACT NUMBER
	5b. GRANT NUMBER
	5c. PROGRAM ELEMENT NUMBER
6. AUTHOR(S)	5d. PROJECT NUMBER
	5e. TASK NUMBER
	5f. WORK UNIT NUMBER
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) **Space and Naval Warfare Systems Center,53560 Hull Street,San Diego,CA,92152-5001**	8. PERFORMING ORGANIZATION REPORT NUMBER
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)	10. SPONSOR/MONITOR'S ACRONYM(S)
	11. SPONSOR/MONITOR'S REPORT NUMBER(S)

12. DISTRIBUTION/AVAILABILITY STATEMENT

Approved for public release; distribution unlimited

13. SUPPLEMENTARY NOTES

The original document contains color images.

14. ABSTRACT

A 64 x 128 real-time infrared (RTIR) complementary metaloxide semiconductor (CMOS)/ silicon-on-insulator (SOI) scene generation integrated circuit (IC) is described. The RTIR IC offers real-time dynamic thermal scene generation. This system is a mixed-mode design, with analog scene information written and stored into a thermal pixel array. The design uses micro-electromechanical sensors (MEMS) in conjunction with SSC San Diego's 0.8-µm CMOS/SOI process to develop a RTIR IC scene generator.

15. SUBJECT TERMS

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			
unclassified	**unclassified**	**unclassified**		**3**	

the pn junctions of the sampling switch and secondarily a result of excessive channel leakage. As an option to further reduce droop, the designer can place a compensation pn junction by using half a negative-channel metal-oxide semiconductor (NMOS) transistor at the hold capacitor node.

FABRICATION

CMOS/MEMS technology is used as a technique to thermally isolate the infrared emitter microstructures from the substrate after the CMOS processing is completed. SSC San Diego's 0.8-µm CMOS partially depleted SOI process was selected to fabricate the array of electronically addressable 20 x 20 micron emitter elements (Figure 2). The process is a single poly, double metal, salicided process with a high-value resistor option of up to 1 Kohm/square. This allows modest density arrays, and, together with the high-value silicon resistor available in the 0.8-µm process, provides lower pixel current operation. The micromachined cavity is constructed by using a silicon etchant that undercuts the desired pattern in the silicon substrate, while leaving it electrically connected to create a suspended structure/microheater (Figure 3). This pattern is created by patterning and plasma etching silicon dioxide after the CMOS passivation, thereby exposing the substrate silicon of the CMOS chip. The exposed silicon is then exposed to a tetra-methyl ammonium hydroxide (TMAH) solution, an aniso-tropic silicon etchant. The TMAH etchant was chosen because, with the addition of silicic acid, it does not attack the exposed aluminum bonding pads [2].

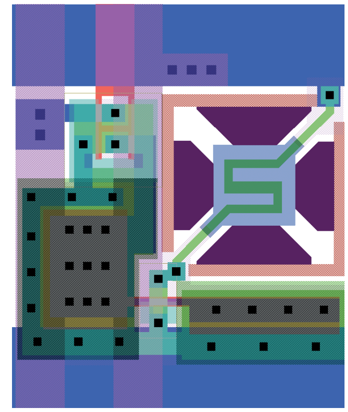

FIGURE 2. The heater element and pixel electronics layout.

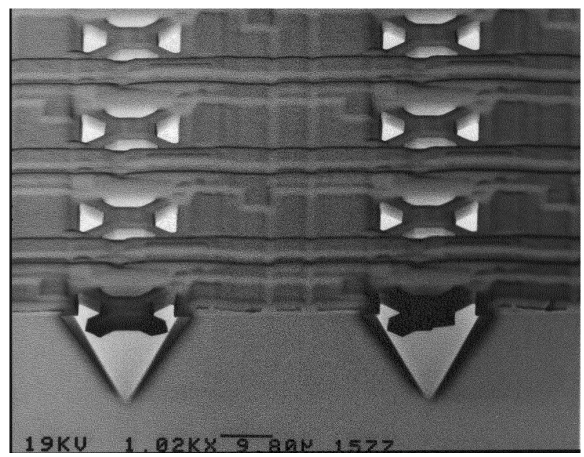

FIGURE 3. Scanning electron microscopy (SEM) of a cross-sectioned sample of suspended microheaters.

RESULTS

The thermally isolated resistor emitter has been characterized using a calibrated blackbody and adjusting for fill factor using a method described in [3]. The temperature of the emitter as a function of voltage across the resistor is plotted in Figure 4, together with the current through the resistor. A maximum temperature of 262°C is achieved at a voltage of 8.25 V and a current of 0.85 mA.

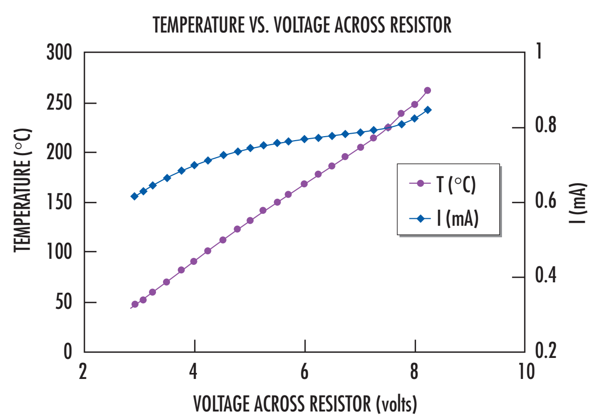

FIGURE 4. Pixel thermal response to applied voltage across resistor.

SUMMARY

A 64 x 128 scene generator RTIR IC architecture has been described with each key component discussed. A MEMS device, the TPA, is produced using CMOS/SOI technology with post CMOS process etching.

ACKNOWLEDGMENTS

This work was funded by the Office of Naval Research, Physical Science Division, Dr. Phil Abraham.

AUTHORS

Bruce Offord

BS in Engineering Physics, University of San Diego, 1985

Current Research: Very large-scale integrated (VLSI) SOI process development; novel IC design.

Richard Bates

BA in Physics, Loma Linda University, 1960

Current Research: Radiation-induced Irtran 2 absorption; polarization independent narrow channel (PINC) wavelength division multiplexing (WDM) fiber coupler fusing.

H. Ronald Marlin

BA in Physics, La Sierra University, 1959

Current Research: Infrared radiometry.

Chris Hutchens

Ph.D. in Electrical Engineering, University of Missouri, 1979

Current Research: Low-power, mixed-signal SOI CMOS and analog CMOS.

Derek Huang

MS in Electrical Engineering, Oklahoma State University, 2001

Current Research: Low-power, mixed-signal SOI CMOS.

Jeremy D. Popp

BS in Electrical Engineering, Portland State University, 1998

Current Research: Low-power, mixed-signal application-specific integrated circuit (ASIC) design; novel systems on a chip; reconfigurable computing.

REFERENCES

1. Parameswaran, M., A. M. Robinson, D. L. Blackburn, M. Gaitan, and J. Geist. 1991. "Micromachined Thermal Radiation Emitter from a Commercial CMOS Process," *IEEE Electron Device Letters*, vol. 12, no. 2 (February), pp. 57–59.
2. Tabata, O., R. Asahi, H. Funabashi, K. Shimaoka, and S. Sugitama. 1992. "Anisotropic Etching of Silicon in TMAH Solutions," *Sensors and Actuators*, A.34, pp. 51–57.
3. Marlin, A. H. R., R. L. Bates, M. H. Sweet, R. M. Carlson, R. B. Johnson, D. H. Martin, R. Chung, J. C. Geist, M. Gaitan, C. D. Mulford, E. S. Zakar, R. J. Zeto, R. Olson, and G. C. Perkins. 1997. "Real-time Infrared Test Set: Assessment and Characterization," *SPIE*, vol. 3084.

❖